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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MCDONALD, RODNEY GLENN	

ART UNIT	PAPER NUMBER
1753	

DATE MAILED: 07/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/781,987	CHA ET AL.	
	Examiner	Art Unit	
	Rodney G. McDonald	1753	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *36-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *36-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 36-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edwards et al. (U.S. Pat. 5,259,881) in view of den Boer et al. (U.S. Pat. 5,641,974) and Zhang et al. (U.S. Pat. 5,578,520).

Edwards et al. teach an apparatus for depositing a layer on a substrate as seen in Fig. 1. Edwards et al. teach in Fig. 1 a cluster tool 10, which includes a front transport module 12 and a back transport module 14. The transport modules 12, 14 are provided with vacuum pumps (not shown) to **maintain their internal chambers at a**

vacuum pressure level suitable for the processing of semiconductor wafers. (Column 5 lines 41-52)

The transport modules 12, 14 are interconnected by an interconnecting conduit and aligner 16 that joins the interiors of the transport modules 12, 14 to form common transport chamber 18 **at a consistent vacuum level and of a common atmosphere**. Within the transport modules 12, 14 is a wafer transport mechanism or robot arm 20 that rotates about a central axis of the respective module 12, 14 and extends through the ports to load and unload single wafers from the adjoining modules, including the processing modules, handling modules and the other transport module. (Column 6 lines 1-11)

The back transport module 14 has six module connection faces or sides for connection to six adjacent modules. On one of these sides is, in the illustrated embodiment, connected a soft etch module 22 for the cleaning or mild etching preconditioning of the surfaces of wafers. A second of these sides is connected to **a first sputter coating module 24, which will typically perform a sputter coating process to deposit a uniform coating on the surface of the wafer**, usually following the soft etch process in the module 22. Another or third side is connected to another processing module, a rapid thermal processing (RTP) module 26, for treating the wafer quickly with high temperatures of, for example 1000.degree. C., to anneal or smooth **a previously deposited coating, such as a metal coating deposited by a sputter coating process in the sputtering module 24**. A forth side is connected to another processing module, for example a sputtering module 28, that may be a sputter etching

module or another sputter coating module. **A fifth face is connected to another processing module 30 that may be, for example, a chemical vapor deposition (CVD) module.** The types of modules and the processes performed therein may be any process suitable to be performed on wafers in conjunction with the other processes being performed by the cluster tool. The sixth face of the transport module is connected to the aligner 16. (Column 6 lines 12-39)

The load-locks 32, 24 each have an access door through which a standard cassette of, for example 25, wafers are held in a rack, usually made of a plastic material such as polypropylene. The racks are loaded and unloaded either manually or by robot through a load-lock access door 41 into each of the load-locks 32, 34. **The access doors 41, when closed, seal internal load-lock chambers within the load-locks so that they may be pumped to the vacuum environment of the transport chamber 18 to permit entry of the wafers, transferred individually by the transport arm 20, into the transport chamber 18 and to the other modules of the cluster tool 10.** When the transport arm 20 returns wafers to the load-locks 32, 34, the load-lock is vented to the external environment. Except when the load-locks are at the vacuum pressure level of the transport chamber 18, the gate valve between the transport chamber 18 and respective load-lock 32, 34 is closed. (Column 6 lines 51-68)

Connected to the other two faces of the entry transport module 12 are two preferably identical batch preheating, degassing or desorbtion **modules 42, 44.** Each of these modules is equipped to receive, hold and preprocess a plurality of wafers

simultaneously, preferably any number up to the quantity held in a full wafer cassette handled by the load-locks 32, 34. (Column 7 lines 1-7)

The batch preheating modules 42, 44 according to certain embodiments of the present invention, will be described in relation to the module 42. Referring to FIG. 2, the preheating module 42 includes a pressure tight housing 50 enclosing a preheating chamber 52. The housing has a hole 53 therein to which a high vacuum pump 54 (removed in this figure; see FIG. 3) is connected to maintain the chamber 52 at a high vacuum, typically equal to that of the transport chamber 18. The module 42 is also conventionally provided with a second pump (not shown) for lowering the pressure from atmospheric pressure to within the operating range of the pump 54, and with a vent port (not shown) for returning the pressure within the chamber 52 to that of the atmosphere. The housing 50 also has therein, on the front thereof, a rectangular port 56 to which the module is connected to a gate valve 58 (FIG. 3) of the front transport module 12. (Column 7 lines 12-25).

The differences between Edwards et al. and the present claims is that utilizing the chambers for forming layers of a thin film transistor is not discussed, the layers of a thin film transistor is not discussed, forming the gate insulating layer, the amorphous silicon layer, the doped amorphous silicon layer and the metal layer without patterning the gate insulating layer, the amorphous silicon layer, the doped amorphous silicon layer is not discussed and depositing the layers in a series of chambers is not discussed.

den Boer et al. teach forming a TFT for an LCD by providing a gate metal layer by sputtering a gate metal layer on a substrate. (Column 7 lines 15-27) The gate metal layer is the dry etched in order to pattern the gate metal layer. (Column 7 lines 33-45) Next a gate insulating layer 21 is deposited over substantially the entire substrate 19 by plasma enhanced CVD or some other process know to produce a high integrity dielectric. Gate insulating layer 21 is preferably silicon nitride but may also be silicon dioxide or other known dielectrics. The gate insulating layer is 2,000-3,000 Angstroms. (Column 46-58) After gate insulating layer 21 has been deposited semiconductor (e.g. intrinsic a-Si) layer 23 is deposited on top of gate insulating layer 21 to a thickness of about 2,000 Angstroms. Semiconductor layer 23 may be from about 1,000 to 4,000 Angstroms. Then, doped (typically phosphorus doped, that is n+) amorphous silicon contact layer 25 is deposited over intrinsic a-Si layer 23 in a known manner to a thickness of, from about 200 to 1,000 Angstroms. (Column 8 lines 3-14) Gate insulating layer 21, semiconductor layer 23 and semiconductor contact layer 25 may all be deposited on substrate 19 in the same deposition chamber without breaking the vacuum according to certain embodiments of this invention. The resulting structure is shown in Figure 9. (Column 8 lines 15-19; Figure 9) Following the formation of the structure of Figure 9, the TFT island or area may be formed by way of etching, for example, so that the TFT metal layers can be deposited thereon. ***Optionally, one of the TFT metal source/drain layers may be deposited before forming the TFT island.*** (Column 8 lines 28-32) The metal layer may be chromium or molybdenum. The metal layer can be 500-2,000 Angstroms. (Column 8 lines 33-44)

The motivation for depositing the metal layer before etching to form the TFT is that it allows for formation of a TFT island structure. (Column 8 lines 28-32)

Zhang et al. teach forming a semiconductor device utilizing a multi-chamber system. (See Abstract) Zhang et al. teach a multi-chamber system for fabricating TFTs on a substrate shown in Fig. 3. The multi-chamber system utilized in this embodiment is a modification of the system shown in Fig. 2 (To be discussed). While the chamber are serially connected in one line in the system of Fig. 2, a plurality of chambers are connected with one another through one common chamber in the present embodiment, as referred to hereinbefore. (Column 7 lines 27-33)

In Fig. 2 the apparatus comprises a serial arrangement for forming the TFT. (Column 6 lines 6-13)

The motivation for continuing to treat the substrate under vacuum in a serially arranged apparatus is that it allows avoiding neutralization of dangling bonds. (Column 6 lines 49-55)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Edwards et al. by depositing in the chambers the layers required for forming a thin film transistor and forming the gate insulating layer, the amorphous silicon layer, the doped amorphous silicon layer and the metal layer without patterning the gate insulating layer, the amorphous silicon layer, the doped amorphous silicon layer as taught by den Boer et al. and to have arranged chambers in serial as taught by Zhang et al. because it allows for layer formation of an island structure and for avoiding neutralization of dangling bonds.

Claims 36-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Turner et al. (U.S. Pat. 5,512,320) in view of den Boer et al. (U.S. Pat. 5,641,974) and Zhang et al. (U.S. Pat. 5,578,520).

Turner et al. teach a method for depositing sequential thin films on glass substrates by single substrate deposition comprising loading a batch of substrates into a load lock chamber and evacuating the chamber, transferring the substrates to a batch heating chamber for heating the substrates to elevated temperatures; transferring the glass substrates singly to one or more single substrate processing chambers, and sequentially transferring the substrates back to the load lock chamber where they are batch cooled. (See Abstract)

Liquid crystal cells for active matrix TV and computer monitors are made of two glass plates sandwiching a layer of liquid crystal material between them. The glass plates are made conductive with a thin conductive film on the inside faces of the plates so that a source of power may be connected to them for changing the orientation of the liquid crystal molecules. As the need for larger and more sophisticated cells that allow separate addressing of different areas of the **liquid crystal cell has progressed**, as for active matrix TV where up to 1,000,000 or more different areas or pixels need to be separately addressed, **the use of thin film transistors for this application has come into widespread use. Thin film transistors comprise a patterned metal gate** over which is deposited a gate dielectric layer and a conductive layer, such as amorphous silicon. **Subsequently applied layers, as of doped amorphous silicon, etch stopper silicon nitride, silicon oxide, metal contact layers and the like, are also required to**

be deposited over the amorphous silicon thin film. Many of these films are deposited by CVD in order to obtain high quality films. (Column 1 lines 15-34)

A vacuum system 10 for processing large glass substrates in accordance with the invention is shown in FIG. 1. The vacuum system 10, referring now to FIG. 1, comprises a central transfer chamber 12 to which are connected **two load lock/cooling chambers 14A and 14B**, each for transferring the glass substrates to be processed into the system 10. The load lock/cooling chambers 14A and 14B have a closable opening comprising a load door 16A and 16B respectively on its outside wall for transfer of glass substrates to be processed into the vacuum system 10 from the atmosphere. (Column 3 lines 19-28)

The cassettes 17 in the load lock/cooling chambers 14 are mounted on an elevator assembly (not shown) to raise and lower the cassettes 17 incrementally the height of one shelf. To load chamber 14A, the load door 16A is opened and one glass substrate is placed on a shelf in the cassette 17. The elevator assembly raises the cassette 17 by the height of one shelf so that an empty shelf is opposite the load door 16A. Another substrate is placed on that shelf and so forth until all of the shelves of the cassette 17 are filled. **At that point the load door 16A is closed and the chamber 14A is evacuated to the desired pressure in the vacuum system 10.** (Column 4 lines 1-11)

A slit valve 20A on the inside wall of the load lock/cooling chamber 14A adjacent to the transfer chamber 12 is then opened. **The glass substrates are transferred by**

means of a robot 22 in the transfer chamber 12 to a heating chamber 28. (Column 4 lines 12-16)

After the last glass substrate is loaded into the heat cassette 29, the first glass substrate has reached processing temperature. **After a heated glass substrate is transferred by means of the robot 22 to one of the single substrate processing chambers 40, 42, 44 and 46, it is always replaced with a cold one to be heated. The processing chambers 40, 42, 44 and 46 are adapted to deposit one or more thin layers onto the glass substrates.** Each of the film chambers 40, 42, 44 and 46 are also fitted on their inner walls 40a, 42a, 44a and 46a respectively with a slit valve 41, 43, 45 and 47 respectively for isolation of the process gases. More than one process chamber can be operational at the same time. (Column 4 lines 46-53)

Although the above system is described using a plurality of film deposition chambers, **other single substrate processing chambers can be included or substituted**, including etch chambers, **physical vapor deposition chambers**, preclean chambers and the like. (Column 5 lines 4-8)

The arrows 48, 49 and 50 respectively show the direction of transfer for one possible sequence; arrow 48 shows the direction of **transfer from the load lock/cooling chamber 14B to the heating chamber 28; arrow 49 shows the direction of transfer of a substrate from the heating chamber 28 to a CVD chamber 40**; and the arrow 50 shows the direction of transfer of a substrate from the CVD chamber 40 back to the load lock/cooling chamber 14B until the load lock is fully exchanged; then when the chamber 14B is venting to atmosphere, load lock

chamber 14A is available to the vacuum robot so that continuous processing is provided. (Column 5 lines 21-31)

For the manufacture of thin film transistors onto large glass substrates, the average time for loading a glass substrate into and unloading it out of a load lock/cooling chamber is about 15 seconds for each operation; (Column 6 lines 18-21).

The differences between Turner et al. and the present claims are that the order and thickness of the layers are not discussed, forming the gate insulating layer, the amorphous silicon layer, the doped amorphous silicon layer and the metal layer without patterning the gate insulating layer, the amorphous silicon layer, the doped amorphous silicon layer and the metal layer is not discussed and depositing the layers in a series of chambers is not discussed.

den Boer et al. is discussed above and teach the order and the thickness of layers for a thin film resistor and forming the gate insulating layer, the amorphous silicon layer, the doped amorphous silicon layer and the metal layer without patterning the gate insulating layer, the amorphous silicon layer, the doped amorphous silicon layer and the metal layer. (See den Boer et al. discussed above)

The motivation for the layers in a certain order, certain thickness and depositing all the layers without patterning is that it allows formation of a LCD with transistors. (See Abstract)

Zhang et al. is discussed above and teach arranging chambers in serial to form a thin film transistor. (See Zhang et al. discussed above)

The motivation for continuing to treat the substrate under vacuum in a serially arranged apparatus is that it allows avoiding neutralization of dangling bonds. (See Zhang et al. discussed above)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Turner et al. by depositing the layers in a certain order, with a certain thickness and depositing all the layers without patterning the layers as taught by den Boer et al. and to have serially arranged vacuum chamber as taught by Zhang et al. because it allows for formation of a LCD with transistors and avoiding neutralization of dangling bonds.

Response to Arguments

Applicant's arguments filed May 6, 2005 have been fully considered but they are not persuasive.

In response to the argument that den Boer does not provide motivation for not etching the gate insulating layer, the semiconductor layer and the semiconductor layer prior to forming the TFT island, it is argued that den Boer teaches either etching or not etching before forming the TFT island. Applicants admit this in their response of May 6, 2005. The motivation for not etching the gate insulating layer, the semiconductor layer and the semiconductor contact layer prior to forming the TFT island is that it allows formation of the TFT structure with the metal film. Also while Applicant has argued that there is no motivation to deliberately not etch the gate insulating layer, the semiconductor layer and the semiconductor contact layer before forming the metal layer, it is argued that den Boer has provided this as an option and that one of ordinary

skill in the art would look to this as a possibility with the motivation being that a TFT is desired to be formed. This motivation would also apply to the case where the etching occurs before metal film formation. (See den Boer discussed above)

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rodney G. McDonald whose telephone number is 571-272-1340. The examiner can normally be reached on M- Th with Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam X. Nguyen can be reached on 571-272-1342. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Rodney G. McDonald
Primary Examiner
Art Unit 1753

RM
June 28, 2005